A GaAs MMIC FOR A 2-7GHz SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER

L.W. Chua

Racal Research Ltd., Walton on Thames,
Surrey, KT12 3PL. United Kingdom.

ABSTRACT

This paper reports on a GaAs MMIC for a successive detection logarithmic amplifier which gives a logging linearity over the instantaneous bandwidth 2-7GHz of ±1.25dB (theory: ±1.1dB). It represents the best published results for both hybrid MIC and MMIC realisations, and the lowest chip count per stage, to date, for frequencies above 2GHz.

INTRODUCTION

Logarithmic amplifier designs for frequencies below 1GHz are well established and find extensive use in radar if amplifiers (Ref. 5). However, for broad instantaneous bandwidth EW systems which require signal processing/detection above 2GHz the conventional detector logarithmic video amplifier has been the standard work horse for a number of years, and its limitations are well known. The RF successive detection logarithmic amplifier (SDLA) as shown schematically in Figure 1 can, in theory, overcome some of these limitations, but requires a tight specification for each rf logging stage and a large number of rf stages in the module. This last constraint lends itself naturally to a MMIC solution.

A number of papers on the design of an SDLA for frequencies above 2GHz have been published (Refs. 1-4) but, currently, only hybrid MIC designs have shown promising performance.

This paper presents results on a GaAs MMIC SDLA with a 2 to 7GHz instantaneous bandwidth. We believe that, to date, it is the best published SDLA performance and lowest chip count per stage usable above 2GHz.

CIRCUIT ARCHITECTURE

The SDLA shown schematically in Figure 1, is made up of a cascade of directional detector cells with integral stage gain. Video outputs from the cells, after application of amplitude weighting, are combined in a summing network. This weighting may be easily determined from the value of the cell gain, the number of cells in cascade and the absolute input power logging range required. This summed output approximates to a logarithmic function of the input power. Deviation of this locus from the linear fit through the cusps is defined as the logging error, the theoretical value of which is a function of the stage gain.

Choice of cell architecture in our design was primarily driven by the necessity to minimise sensitivity to active device parameter spreads. Also, interport isolation and impedance match must be relatively independent of input power level.

The cell gain chosen in the current design is 10dB over 2 to 6GHz. This value introduces a theoretical logging error of ±1.25dB. In order that the overall SDLA logging error is primarily determined by this value, a gain ripple of 0.2dB was specified for the cell design.

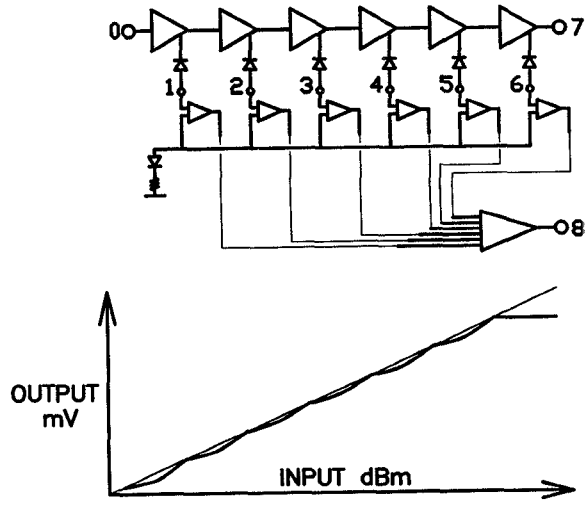

Figure 1 6 Stage SDLA

Figure 2 shows the layout of the MMIC cell. Following pre-amplification and reactive power splitting, the second subcell performs both impedance transformation and reverse isolation.

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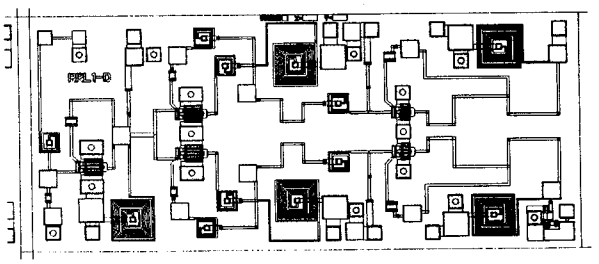


Figure 2 Mask Layout of Cell

The third subcell sets the output power limiting level. A Schottky Barrier detector diode terminates one of the cell outputs. 300 and 600 micron gate periphery MESFETs are employed in parallel feedback configuration for gain slope correction and impedance matching. Theoretical performance of the chip is shown in Figure 3. Due to the close performance tolerance required, measured rather than modelled foundry element data were used wherever possible. The passband gain slope arose from a modelling error in the version of Touchstone used in the design phase. Fabrication of the MMIC chips was carried out at the GEC-Marconi, Caswell, GaAs foundry under the F20 0.5 micron process.

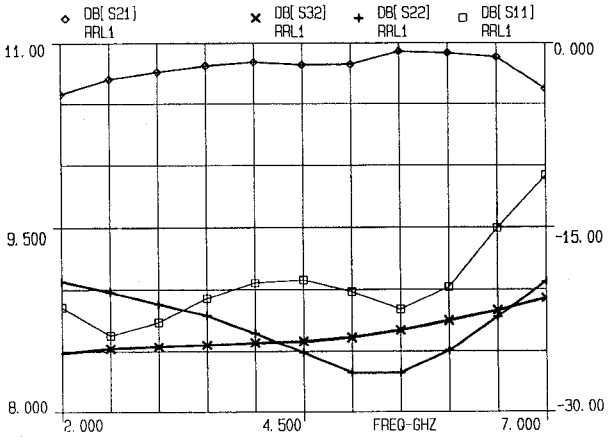
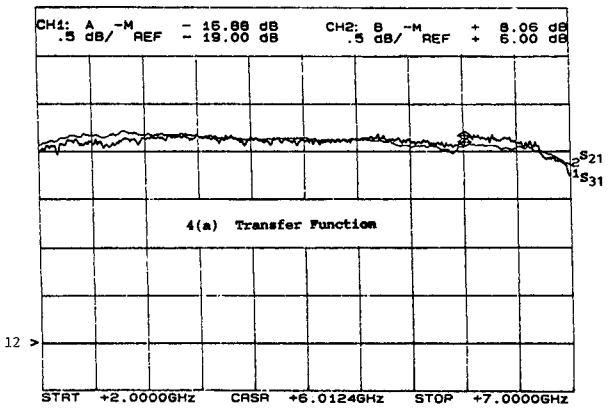


Figure 3 Theoretical Performance of Cell

RESULTS

Figure 4 displays the measured performance of a typical cell. Apart from the reduction in gain, the transfer characteristics are almost identical to that of the theoretical values, and the return losses, after connector de-embedding, are within 1dB of the design values. Tracking and flatness with frequency of the rf and video outputs are within ±0.1dB over a band greater than the 2 - 7GHz frequency window. Reverse isolation (not shown) is in excess of 40dB.



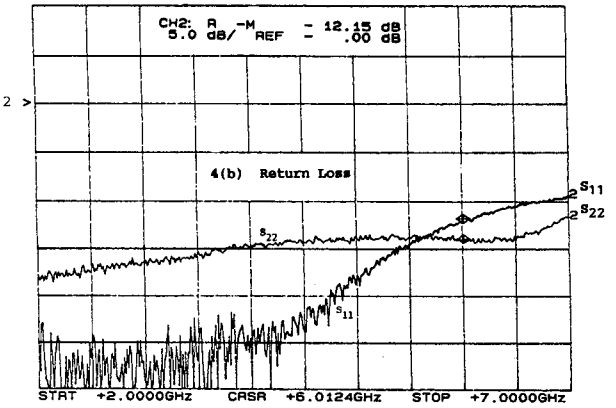


Figure 4 Measured Performance of Cell

In the evaluation of the six cell structure shown in Figure 5, the gate bias has been increased to obtain a cell gain of 9dB. Figure 6 shows the swept frequency performance of the six cell cascade. The output trace numbers correspond to the cell outputs indicated in Figure 1. With the exception of output 7, which represents the rf output at port 7, all traces show normalised video outputs from the integral detectors. These traces are almost identical to that predicted from data measured individually on the cells before module assembly. Overall gain in the linear region over the frequency band 2 to 7GHz is 52.6 ± 0.6dB. As each cell progressively saturates, no significant perturbation to the adjacent cells is introduced. It can be seen in Figure 6 that the rf output remains at +10dBm ± 2.5dB over at least a 40dB dynamic range in the 2 to 7GHz frequency window, demonstrating the good rf limiting amplifier property.

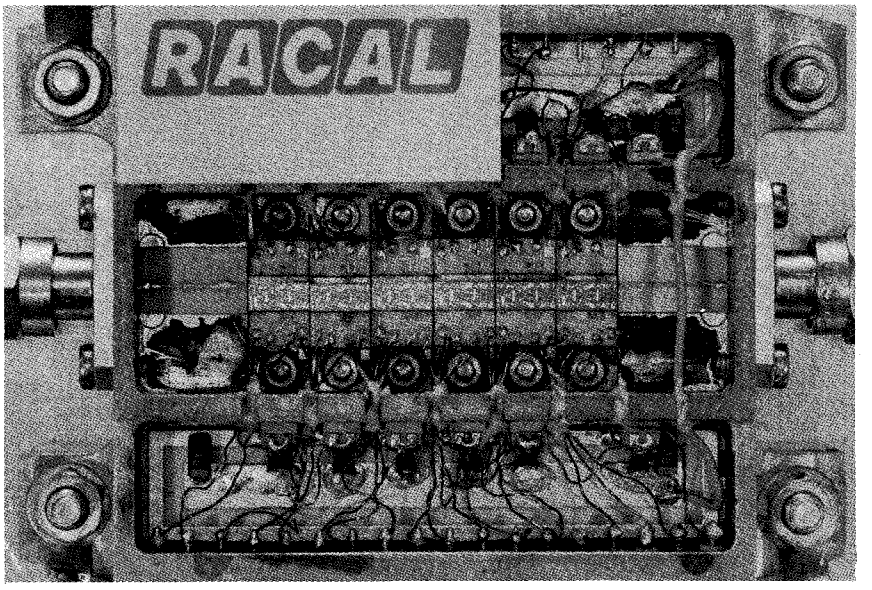


Figure 5 6 Stage SDLA Module

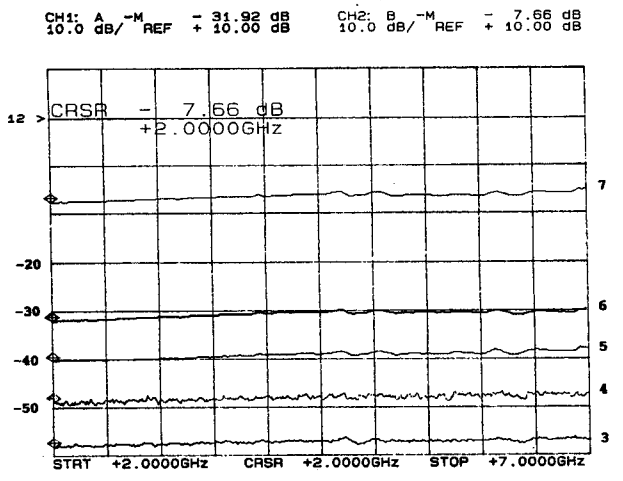


FIGURE 6a 6 STAGE PERFORMANCE: PIN -60dBm

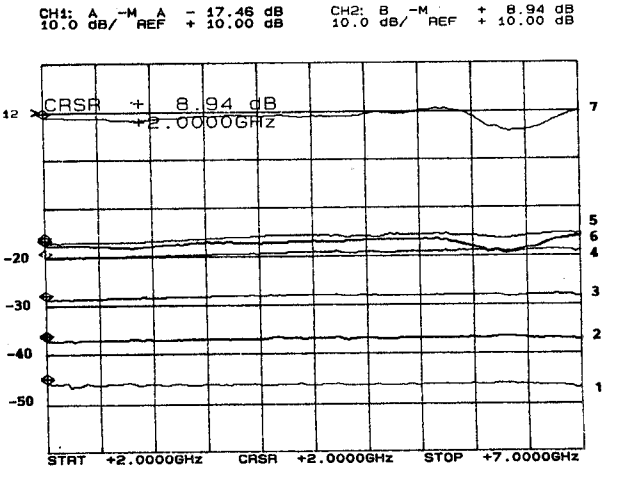


FIGURE 6b 6 STAGE PERFORMANCE: PIN -30dBm

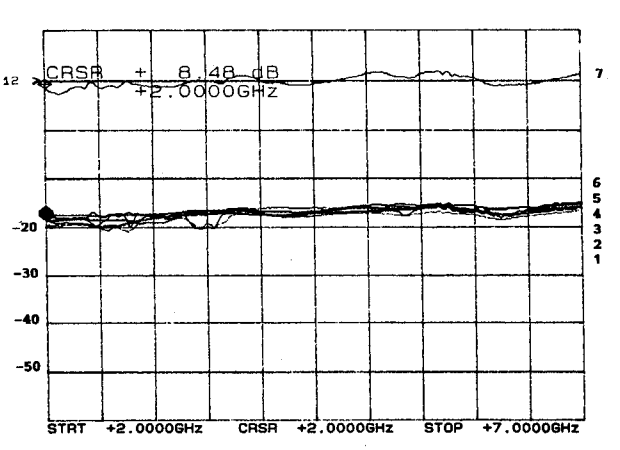


FIGURE 6c 6 STAGE PERFORMANCE: PIN +7dBm

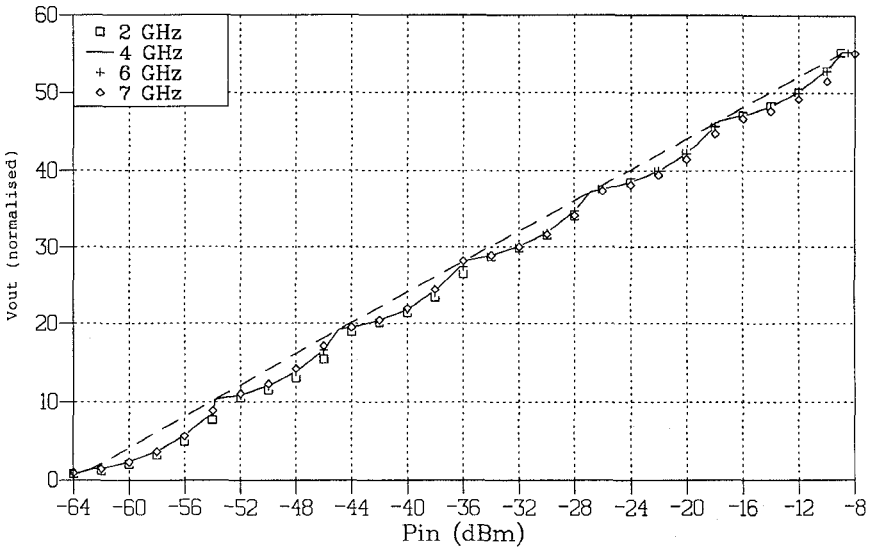


Figure 7 6 Stage SDLA

Figure 7 shows the measured transfer characteristics of the module operating as a six stage SDLA. Logging error over the 54dB dynamic range is ±1.25dB within the 2 to 7GHz instantaneous frequency window. This is very close to the theoretical value of ±1.1dB for a 9dB stage gain. The above results represent the best published figures and lowest chip count per stage for both hybrid MIC and MMIC realisations of an SDLA above 2GHz, let alone the instantaneous frequency window 2 to 7GHz.

CONCLUSION

A six chip SDLA operating over the frequency band 2 to 7GHz with logging error within ±1.25dB over 54dB dynamic range has been demonstrated. The above excellent performance has been achieved without any post design rf circuit tuning.

A summary of the measured performance at 31°C of the module is tabulated below.

Instantaneous bandwidth	2-7GHz
Dynamic Range	54dB
Logging error	±1.25dB
Max. input and output vswr over dynamic range	1.5:1
Small signal rf gain of module	52.6 ± 0.6dB
rf output level over a minimum of 40dB dynamic range	+10dBm ± 2.5dB

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